Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1 (Currently Amended). A computer firmware program updating system having a communication function comprising:

a first processor which operates by referring to a firmware program stored ~~therein~~ in a flash ROM; and

a second processor which monitors an operation of said first processor and executes update of said firmware program by using said communication function with an external unit, and executes an update control of said program when a fault of said first processor is detected.

2 (Previously Presented). The program updating system having the communication function according to claim 1,

wherein said second processor transmits a reset signal to said first processor for every predetermined number of cycles, and monitors a response pulse which is transmitted from said first processor in response to said reset signal, and transmits a compulsory reset signal to said first processor when said response pulse can not be detected within a predetermined period.

3 (Previously Presented). The program updating system having the communication function according to claim 2, further comprising:

an activation pulse generating circuit which generates an activation pulse to activate said second processor,

wherein said second processor starts transmitting said reset signal in response to said activation pulse outputted from said activation pulse generating circuit.

4 (Currently Amended). The program updating system having the communication function according to claim 3, further comprising:

a buffer which transiently stores ~~said~~ a program to be used for executing said firmware program update ~~control~~, wherein said second processor transfers said program stored in said buffer to said first processor for writing into said flash ROM, after an operation of storing said program in said buffer is completed.

5 (Currently Amended). The program updating system having the communication function according to claim 1, further comprising:

an activation pulse generating circuit which generates an activation pulse to activate said second processor,

wherein said second processor starts transmitting ~~said~~ a reset signal to said first processor in response to said activation pulse outputted from said activation pulse generating circuit.

6 (Currently Amended). The program updating system having the communication function according to claim 5, further comprising:

a buffer which transiently stores ~~said~~ a program for executing said firmware program update ~~control~~, wherein said second processor transfers said program stored in said buffer to said first processor for writing into said flash ROM, after an operation of storing said program to said buffer is completed.

7 (Currently Amended). The program updating system having the communication function according to claim 1, further comprising:

a buffer which transiently stores ~~said~~ a program for executing said firmware program update ~~control~~, wherein said second processor transfers said program stored in said buffer to said first processor for writing into said flash ROM, after an operation of storing said program to said buffer is completed.

8 (Original). The program updating system having the communication function according to claim 2, further comprising:

an activation monitoring circuit which generates an activation pulse to activate said second processor and monitors transmission of an activation response pulse which is outputted from said second processor in response to said activation pulse,

wherein said activation monitoring circuit transmits a compulsory reset signal to said second processor when said activation response pulse can not be detected within the predetermined period.

9 (Currently Amended). The program updating system having the communication function according to claim 8, further comprising:

a buffer which transiently stores ~~said~~ a program for executing said firmware program update ~~control~~, wherein said second processor transfers said program stored in said buffer to said first processor for writing into said flash ROM, after an operation of storing said program to said buffer is completed.

10 (Currently Amended). The program updating system having the communication function according to claim 1, further comprising:

an activation monitoring circuit which generates an activation pulse to activate said second processor and monitors transmission of an activation response pulse outputted from said second processor in response to said activation pulse,

wherein said activation monitoring circuit transmits a compulsory reset signal to said second processor when said activation response pulse can not be detected within ~~the~~ a predetermined period.

11 (Currently Amended). The program updating system having the communication function according to claim 10, further comprising:

a buffer which transiently stores ~~said~~ a program for executing said firmware program update ~~control~~, wherein said second processor transfers said program stored in said buffer to said first processor for writing into said flash ROM, after an operation of storing said program to said buffer is

completed.

12. (Currently Amended) A computer firmware program updating method using a communication function, comprising:

providing a first processor which operates by referring to a firmware program stored ~~therein~~ in a flash ROM and a second processor;

transmitting a reset pulse from said second processor to said first processor;

transmitting a response pulse from said first processor to said second processor in response to said reset signal which is outputted from said second processor; and

transmitting a compulsory reset signal from said second processor to said first processor to stop an operation of said first processor when said response pulse can not be detected within a predetermined period.

13 (Currently Amended). The program updating method using the communication function according to claim 12, ~~wherein~~ further comprising:

transferring by said second processor ~~transfers said~~ a program obtained by using said communication function to said first processor for writing into said flash ROM, during a stop of said first processor.

14 (Currently Amended). The program updating method using the communication function according to claim 13, further comprising:

providing an activation control circuit which controls activation and a stop of said second processor,

~~wherein~~ transmitting by said second processor ~~transmits~~ an activation response pulse to said activation control circuit for every predetermined number of cycles, and

executing by said activation control circuit ~~executes~~ a stop control of said second processor, when said activation response pulse can not be detected within a predetermined period.

15 (Currently Amended). The program updating method using the communication function according to claim 12, further comprising:

providing an activation control circuit which controls activation and a stop of said second processor~~, wherein~~;

transmitting by said second processor ~~transmits~~ an activation response pulse to said activation control circuit for every predetermined cycles~~;~~; and

executing by said activation control circuit ~~executes~~ a stop control of said second processor, when said activation response pulse can not be detected within a predetermined period.